

LEARNING OUTCOMES

After studying this chapter, you will be able to understand the following:

- Minimum and maximum mode operation of an 8086-based system
- Function of the clock generator (8284A) and the bus controller (8288)
- Bus timings, interrupt acknowledgement, and bus request and grant in the 8086

18.1 INTRODUCTION

To adapt to different situations, the 8086 processors can be operated either in the minimum or the maximum mode. The minimum mode is used for a small system with a single processor (8086) and in any system in which the 8086 generates all the necessary bus control signals directly, thereby minimizing the required bus control logic. The maximum mode is for medium to large size systems, which often include two or more processors. In the maximum mode, the 8086 encodes the basic bus control signals into three status bits (S_2 , S_1 , and S_0) and uses the remaining control pins to provide the additional information that is needed to support the multiprocessor configuration.

18.2 8086 IN MINIMUM MODE CONFIGURATION

The 8086 is configured in minimum mode when its MN/\overline{MX} pin is connected to +5 V. A typical minimum mode configuration of the 8086 is shown in Fig. 18.1. The figure illustrates the 8284 IC generating the clock, Ready and Reset signals for the 8086. The decoder is used to generate the four control signals \overline{MEMR} , \overline{MEMW} , \overline{IOR} , and \overline{IOW} using the M/\overline{IO} , \overline{RD} , and \overline{WR} signals of the 8086. The chip select (CS) logic is used to generate the Chip Select signals for the odd and even memory banks of the RAM and ROM chips and the I/O devices using \overline{BHE} , A_0 , and a few higher-order address lines of the 8086. The \overline{CSE} and the \overline{CSO} signals represent the Chip Select signal for the even bank and odd bank of the memory, respectively. \overline{CSIO} represents the Chip Select signal for the input/output (I/O) devices.

The address from the 8086 and the \overline{BHE} signals are latched externally using three 74LS373 (octal latch) ICs, since they are available only during the first part of the bus cycle. The ALE signal of the 8086 is used to indicate that the bus contains a valid address and is connected to the G or CLK input of the 74LS373 as shown in Fig. 18.2.

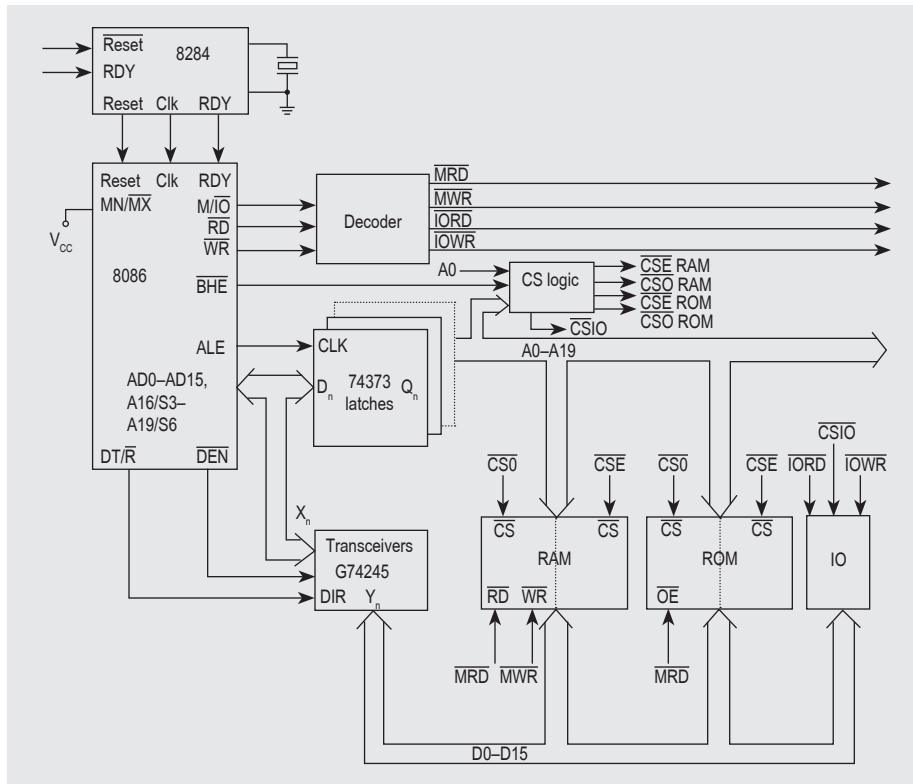


Fig. 18.1 Minimum mode operation of an 8086-based system

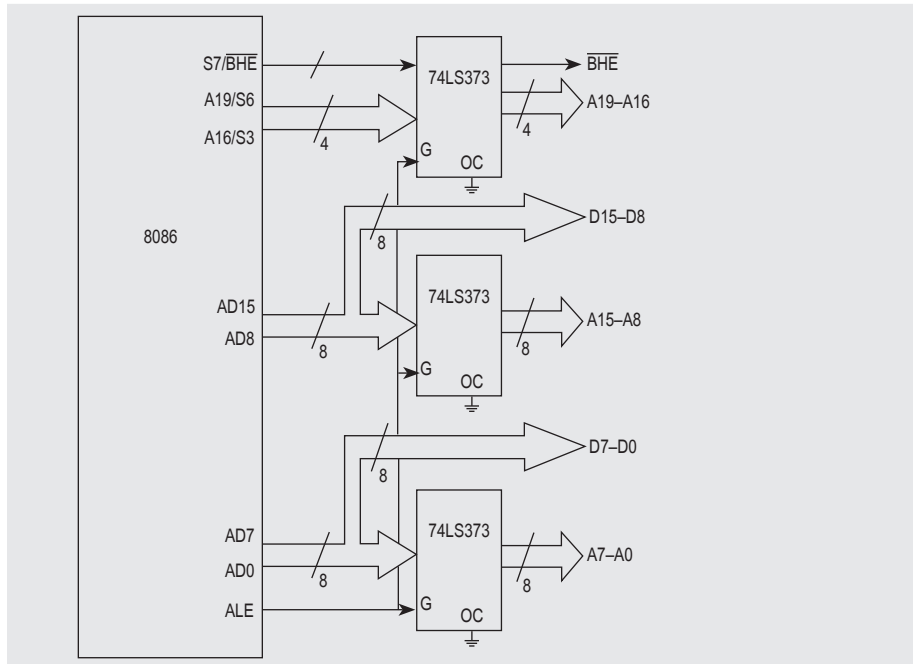


Fig. 18.2 Formation of separate address bus (A19–A0) and data bus (D15–D0) in the 8086

the 74245 is tied to the processor's DT/\overline{R} pin. The processor floats (tri-states) the \overline{DEN} and the DT/\overline{R} pins, in response to a bus request on the HOLD pin. Similarly, three 74244 ICs (buffer/driver) are used to generate the buffered address bus (BA0–BA19), as shown in Fig. 18.3. The Intel 8282 IC and the Intel 8286 IC can be used instead of the 74LS373 and the 74245, respectively.

18.2.3 Connection of 8284A with 8086

Figure 18.4(a) shows the clock generator IC (8284A), which supplies a train of pulses at a constant frequency to the 8086. The connection of the 8284A with the 8086 is shown in Fig. 18.4(b). It synchronizes the Ready (RDY) signal (which indicates that an I/O device or memory interface is ready to complete a data transfer) received from an I/O or memory interface, by activating the READY input of the 8086 at the right time in a bus cycle. Similarly, when the Reset (\overline{RES}) signal of the 8284A is activated, it activates the RESET input of the 8086 at the right time in a bus cycle, which initializes the 8086 system. The clock pulse source applied to the 8284A may be from a pulse generator that is connected to the EFI

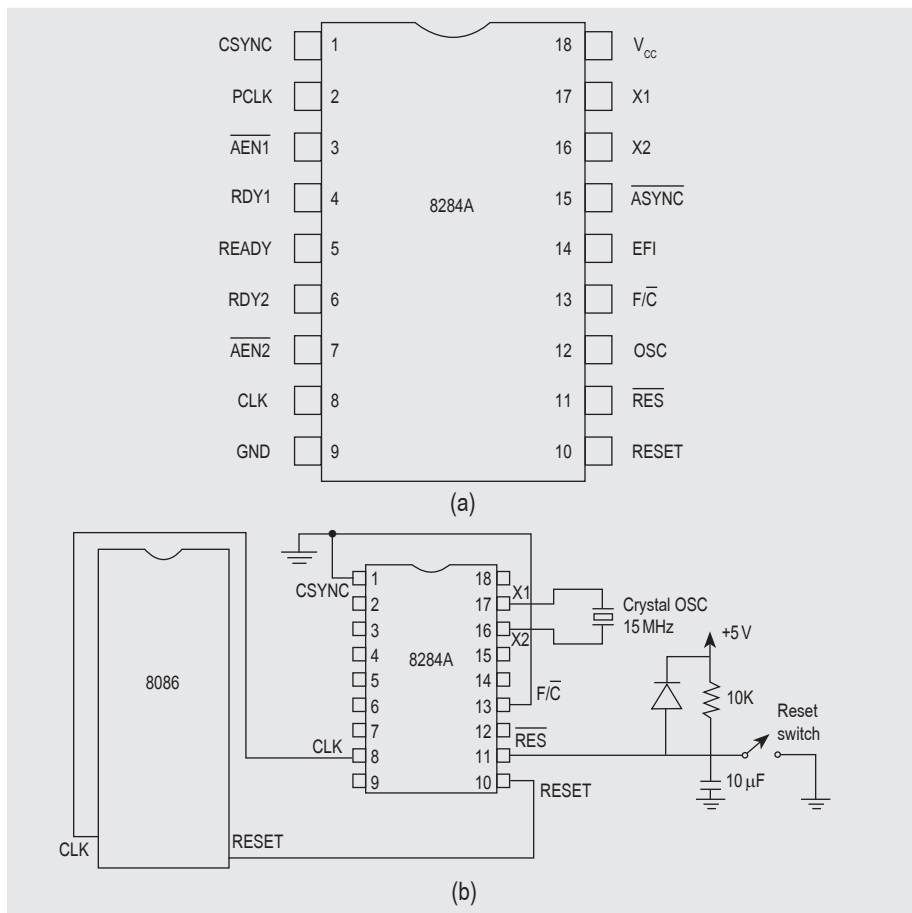


Fig. 18.4 8284 connection diagram (a) Pin details of the 8284A (b) Typical 8284A connection with the 8086

pin or an oscillator that is connected across X1 and X2. If the input to F/\overline{C} is 1, the EFI input determines the frequency. Otherwise, the oscillator input determines the frequency. In either case, the 8284 clock output (CLK) is one-third of the input frequency. All the devices, 74373, 74245, and 8284A, require only +5 V supply voltage. Their inputs and outputs are TTL-compatible and therefore the devices are compatible with each other and with the 8086. CSYNC is used in systems with multiple processors.

In the minimum mode system, the control lines (\overline{RD} , \overline{WR} , and M/\overline{IO}) need not be passed through transceivers, but can be used directly. The \overline{RD} , \overline{WR} , and M/\overline{IO} lines indicate the type of data transfer, as shown in Table 18.1.

Since the content of CS and IP are FFFFH and 0000H after reset, the first instruction for execution is fetched from the memory address FFFF0H (= CSX10H + IP) by the 8086. Hence, the system start-up program must be stored from the address FFFF0H in the memory. Normally, this address is assigned to a ROM-type memory chip, so that the system start-up program is available permanently. The interrupt vector table is stored from the address 00000H in the memory, whenever the interrupt(s) is (are) to be used in the 8086-based system. In addition, depending upon the system requirement, specific interfacing ICs can be used along with the 8086.

- (i) For interfacing the keyboard and the seven-segment display with the 8086, the 8279 IC can be used.
- (ii) To increase the number of hardware interrupts that can be handled by the 8086, the 8259 IC can be used.
- (iii) To interface I/O devices such as DIP switches, ADCs, DACs, LEDs, relays, and stepper motors with the 8086, the 8255 IC is used.
- (iv) For performing serial communication, the 8251 IC is used with the 8086.

18.3 8086 IN MAXIMUM MODE CONFIGURATION

The 8086 operates in the maximum mode when its MN/\overline{MX} pin is grounded. A typical maximum mode configuration is shown in Fig. 18.5. The main difference between the minimum and the maximum mode configuration is the need for additional circuitry to interpret the control signals of the 8086. This additional circuitry accepts the status signals $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ from the 8086 and generates the I/O- and memory-related control signals. It also generates the signals for controlling the external latches (74373) and transceivers (74245).

It is normally implemented with an Intel 8288 bus controller IC. In addition, a programmable interrupt controller (8259) is included in the system. However, its presence is optional.

The $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ status bits specify the type of transfer that is to be carried out by the 8086 and when used with an 8288 bus controller, they are used to generate the memory-, I/O-, and interrupt-related control signals. From the status

Table 18.1 Function of the 8086 control signals in minimum mode operation

M/\overline{IO}	\overline{RD}	\overline{WR}	Operation
0	0	1	I/O read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write

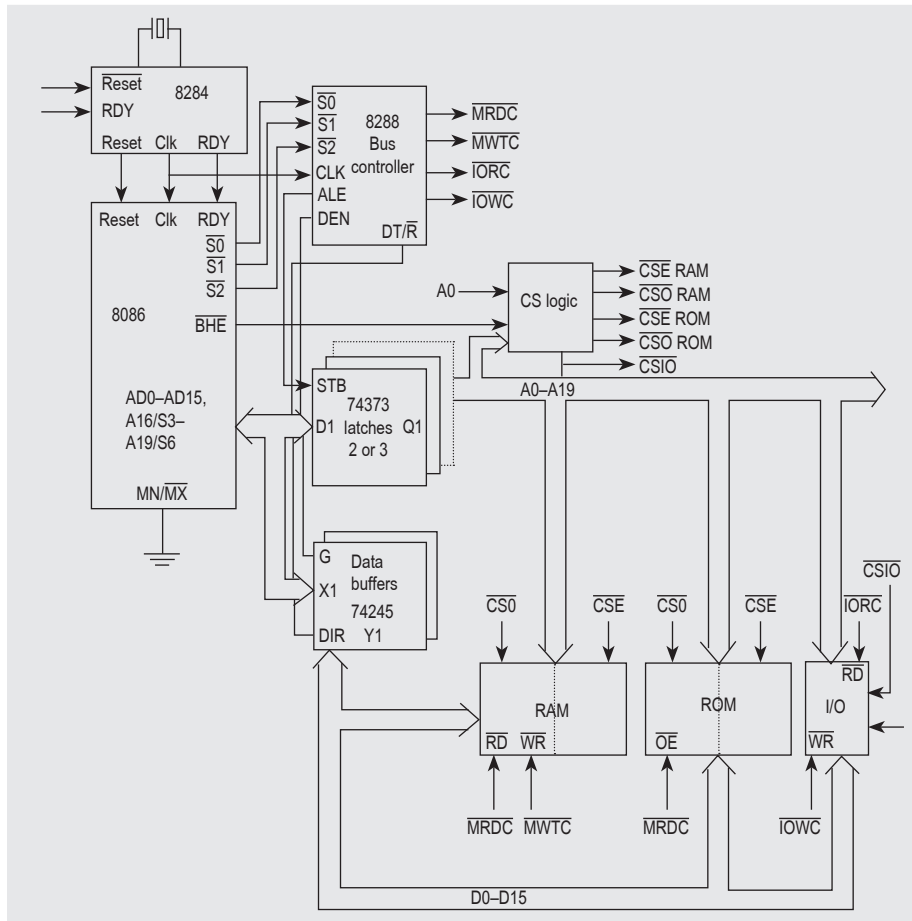


Fig. 18.5 Maximum mode operation of an 8086-based system

bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$, the 8288 is able to generate the Address Latch Enable (ALE) signal for the 74LS373s, the enable and direction signals for the 74245 transceivers, and the Interrupt Acknowledge signal (\overline{INTA}) for the interrupt controller 8259. The QS0 and QS1 pins of the 8086 allow a system external to the 8086 processor such as the 8087 (coprocessor) to know the status of the processor instruction queue, so that it can determine which instruction is currently executed by the 8086. The \overline{LOCK} pin indicates that an instruction with a LOCK prefix is being executed and that the bus is not to be used by another master. These pins are needed only in multiprocessor systems.

The HOLD and HLDA pins become the bus request and the bus grant ($\overline{RQ/GT0}$ and $\overline{RQ/GT1}$) pins in the maximum mode. Both bus requests and bus grants can be given through these pins. Both the pins function in exactly the same way, except that if requests are seen on both the pins at the same time, the one on $\overline{RQ/GT0}$ is given higher priority. A request consists of an active low pulse arriving before the start of the current bus cycle. The grant is an active low pulse that is issued at the beginning of the current bus cycle provided that

- (i) the previous bus transfer in the 8086 was not the lower-order byte of a word to or from an odd address,
- (ii) the first low pulse of an interrupt acknowledgement ($\overline{\text{INTA}}$) did not occur during the previous bus cycle, and
- (iii) an instruction with a LOCK prefix is not being executed.

If condition (i) or (ii) is not met, the grant is not given until the next bus cycle; if condition (iii) is not met, the grant waits until the locked instruction is completed. In response to the grant, the tri-state pins of the 8086 (i.e., address, data, and control pins) are placed in their high impedance state and the next bus cycle is given to the requesting master. The processor is effectively disconnected from the system bus until the master sends a second pulse to the processor through the $\overline{\text{RQ/GT}}$ pin.

The ALE, $\text{DT}/\overline{\text{R}}$, DEN, and $\overline{\text{INTA}}$ pins provide the same outputs that are sent by the 8086 processor when it is in minimum mode (except that DEN is inverted). The CLK input permits the bus controller activity to be synchronized with that of the 8086 processor. The remaining pins given in Fig. 18.5 have the following functions:

- (i) $\overline{\text{MRDC}}$ (memory read command)—This signal instructs the memory to place the contents of the addressed location on the data bus.
- (ii) $\overline{\text{MWTC}}$ (memory write command)—This signal instructs the memory to accept the data on the data bus and place the data in the addressed memory location.
- (iii) $\overline{\text{IORC}}$ (I/O read command)—This signal instructs an I/O interface to place the data contained in the addressed port on the data bus.
- (iv) $\overline{\text{IOWC}}$ (I/O write command)—This signal instructs an I/O interface to accept the data on the data bus and place the data in the addressed port.
- (v) $\overline{\text{INTA}}$ (Interrupt Acknowledge)—This signal is used to send two interrupt acknowledgement pulses to an interrupt controller such as the 8259 or an interrupting device, when $\overline{\text{S0}} = \overline{\text{S1}} = \overline{\text{S2}} = 0$.

These five signals are active low and are outputted during the middle portion of a bus cycle. Only one of them is issued during a bus cycle. There are two more signals— $\overline{\text{AIOWC}}$ (advanced I/O write command) and $\overline{\text{AMWC}}$ (advanced memory write command). They do the same function as the $\overline{\text{IOWC}}$ and $\overline{\text{MWTC}}$ pins. However, they are activated one clock pulse earlier. This gives slow interfaces an extra clock cycle to prepare for accepting the input data. The 8288 requires +5 V power supply and has TTL-compatible inputs and outputs.

18.4 8086 SYSTEM BUS TIMINGS

This section discusses the timing diagram of the 8086 bus cycles—general bus operation, memory and I/O read cycle, memory and I/O write cycle in minimum mode operation, and memory and I/O read cycle and memory and I/O write cycle in maximum mode operation. It also discusses the timing diagram for interrupt acknowledgement ($\overline{\text{INTA}}$) and the bus request and bus grant timing in minimum and maximum mode operation.

18.4.1 Timing Diagrams for General Bus Operation in Minimum Mode

The 8086 bus cycles are depicted with their T-states in Fig. 18.6. The length of a bus cycle in an 8086 system is four clock cycles, denoted by T1–T4, plus any number of wait state clock cycles, denoted by TW. If the bus is to be inactive or idle after the completion of a bus cycle, the gap between successive bus cycles is filled with idle state clock cycles denoted by TI. During data transfer, the wait states are inserted between T3 and T4, when a memory or I/O interface is not able to respond quickly.

The timing diagram for general bus operation of the 8086 in minimum mode is shown in Fig. 18.7. If the Ready signal is still in low state at the beginning of T3, one or more wait states (TW) will be inserted between T3 and T4, until a Ready has been received (i.e., Ready is made 1). The bus activity during TW is the same as the activity during T3. A signal applied to an RDY input of the 8284A causes a Ready output to the 8086 at the falling edge of the current clock cycle.

The simplified timing diagram for the memory or I/O read cycle, which requires one wait state in the minimum mode is shown in Fig. 18.8.

The simplified timing diagram for the memory or I/O write cycle, which requires one wait state in the minimum mode is shown in Fig. 18.9.

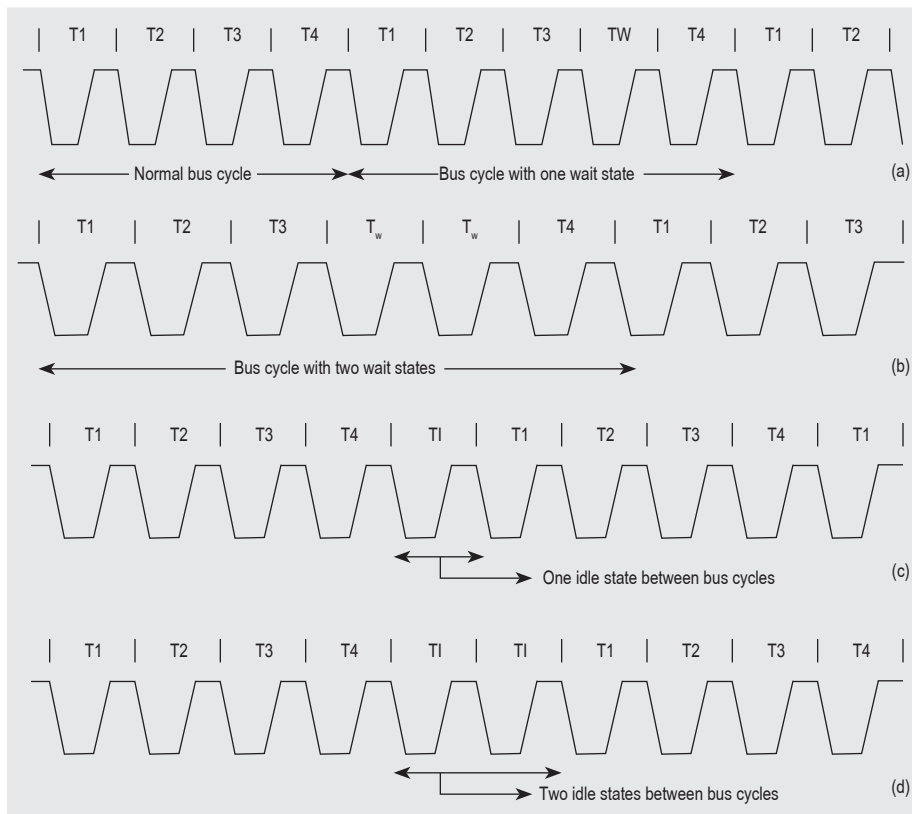


Fig. 18.6 8086 bus cycles (a) Normal bus cycle and bus cycle with one wait state (b) Bus cycle with two wait states (c) Bus cycle with one idle state, and (d) Bus cycle with two idle states

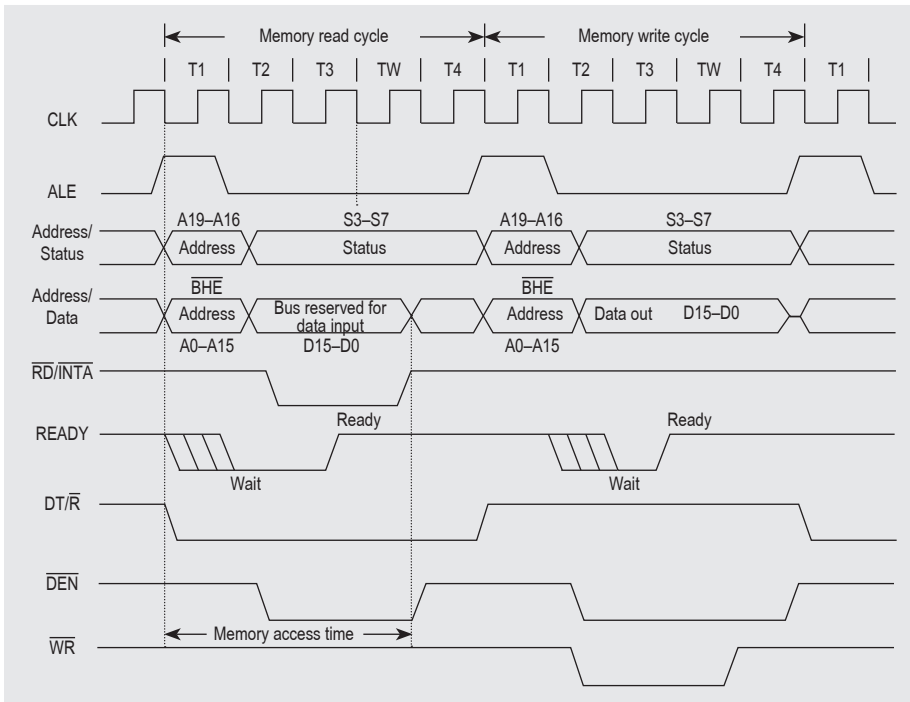


Fig. 18.7 Timing diagram for general bus operation of the 8086 in minimum mode

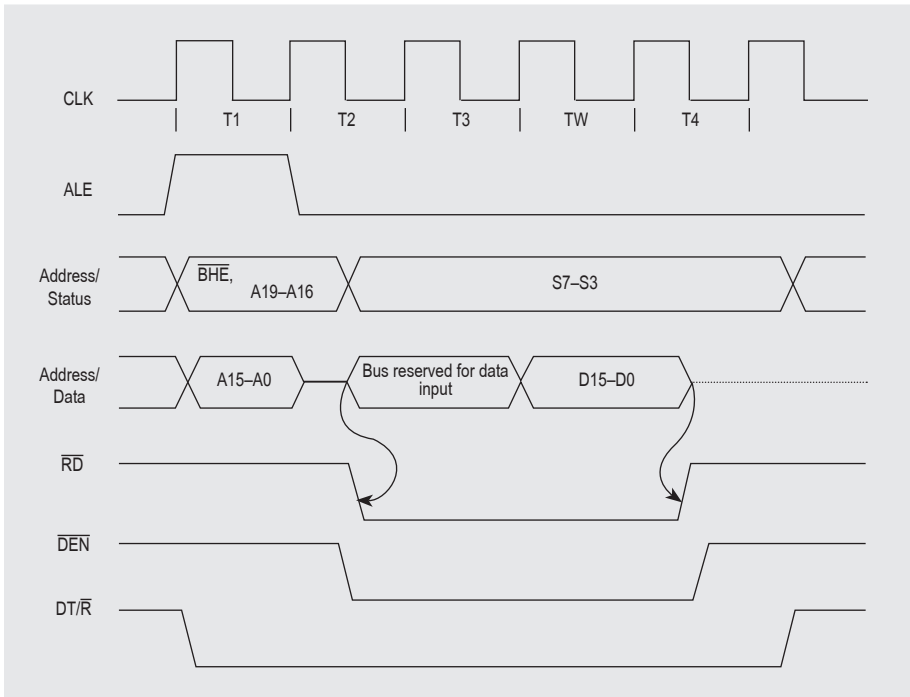


Fig. 18.8 Memory or I/O read cycle in minimum mode operation of the 8086

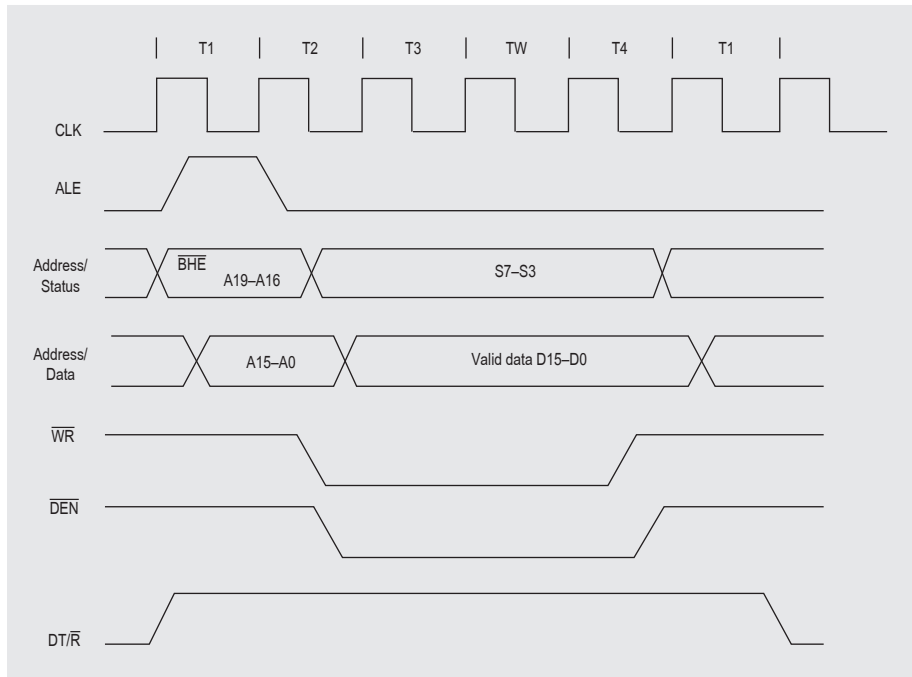


Fig. 18.9 Memory or I/O write cycle in minimum mode operation of the 8086

When the processor is ready to initiate a bus cycle, it places the address in the lines AD15–AD0 and A19/S6–A16/S3, and the status of $\overline{\text{BHE}}$ in the line $\overline{\text{BHE}}/\text{S7}$, and applies a pulse to the ALE pin during T1. Before the falling edge of the ALE signal, the signals in the address lines $\overline{\text{DEN}}$, $\text{DT}/\overline{\text{R}}$, $\text{M}/\overline{\text{IO}}$, and $\overline{\text{BHE}}$ are made stable (i.e., the appropriate value, 1 or 0, is placed on the address lines), with $\text{DT}/\overline{\text{R}} = 0$ for the read operation, and $\text{DT}/\overline{\text{R}} = 1$ for the write operation. At the falling edge of the ALE signal, the 74LS373s latches the address in the lines AD15–AD0 and A19/S6–A16/S3, and the status of $\overline{\text{BHE}}$ in the line $\overline{\text{BHE}}/\text{S7}$. During T2, the address in these lines is removed and the status signals S3–S7 are outputted on the A16/S3–A19/S6 and $\overline{\text{BHE}}/\text{S7}$ pins. $\overline{\text{DEN}}$ is made logic 0 to enable the 74LS245 transceivers. The logic value in the line $\text{M}/\overline{\text{IO}}$ (which is not shown in Figs 18.7, 18.8, and 18.9) is 1 for memory-related operations and 0 for I/O-related operations.

If an input operation (i.e., read operation) is to be performed, $\overline{\text{RD}}$ is active low during T2, and the AD15–AD0 pins should enter a high impedance state in preparation for the receiving of input data. If the memory or I/O interface is ready to transfer data immediately, there are no wait states and the data is put on the bus during T3. After the input data is accepted by the 8086, $\overline{\text{RD}}$ is raised to 1 at the beginning of T4, and the memory or I/O interface removes its data upon detecting this transition.

For an output operation (i.e., write operation), the 8086 makes the signal $\overline{\text{WR}} = 0$ and places the output data in the pins AD15–AD0 during T2. During T4, $\overline{\text{WR}}$ is made logic 1 and the data is removed.

For both input and output operation, $\overline{\text{DEN}}$ is made logic 1 during T4, to disable the transceivers. The $\text{M}/\overline{\text{IO}}$ signal is set according to the next data transfer at this time.

The bus timing of the 8086 has been designed such that the memory or I/O interface involved in a data transfer can control when data is to be placed on or taken from the bus by the interface. This is done by having the interface send a Ready signal to the 8086 (via the 8284), when it has placed data on the data bus or has accepted data from the data bus.

18.4.2 Timing Diagrams for General Bus Operation in Maximum Mode

The timing diagram for the memory or I/O read cycle without any wait state, in a maximum mode 8086 system, is shown in Fig. 18.10.

The timing diagram for the memory write cycle without any wait state, in a maximum mode 8086 system, is shown in Fig. 18.11. The status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are set just prior to the beginning of the bus cycle. Upon detecting a change from the passive state ($\overline{S0} = \overline{S1} = \overline{S2} = 1$), the 8288 outputs a pulse on its DT/ \overline{R} pin during T1. In T2, the 8288 sets $DEN = 1$, thus enabling the transceivers. For memory read operation, it activates \overline{MRDC} , which is maintained until the end of the clock period T4. For a memory write operation, \overline{AMWC} is activated from T2 to T4 and \overline{MWTC} is activated from T3 to T4. The status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ remain active until the end of T3 and become passive (all 1s) during T3 and T4. As with the minimum mode, if the Ready input of the 8086 is not activated before the beginning of T3, the wait states are inserted between T3 and T4.

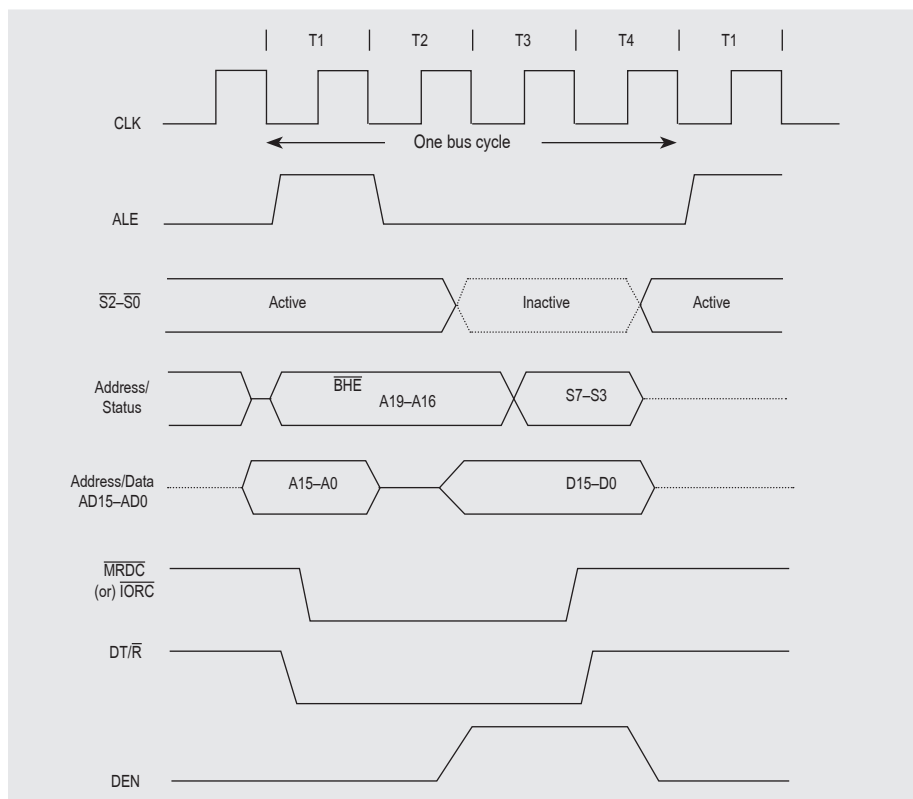


Fig. 18.10 Memory or I/O read cycle in maximum mode operation of the 8086

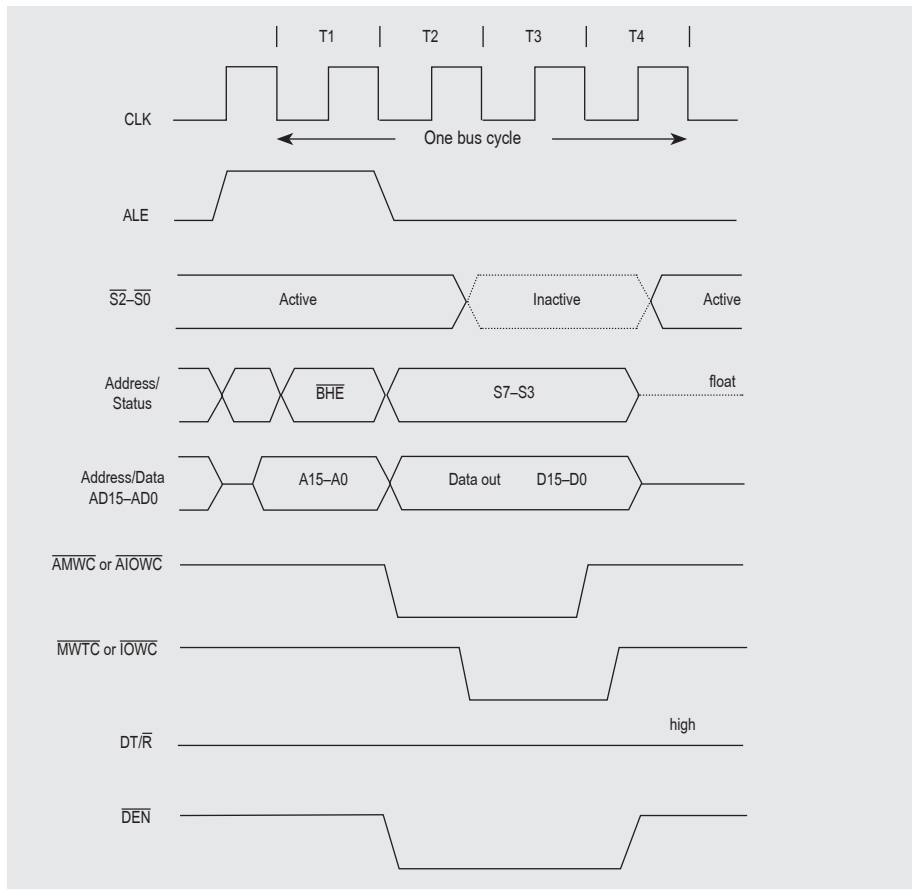


Fig. 18.11 Memory or I/O write cycle in maximum mode operation of the 8086

Similar to the memory read cycle, while performing the I/O read cycle, the control signal $\overline{\text{IORC}}$ is activated instead of $\overline{\text{MRDC}}$. Similar to the memory write cycle, while performing the I/O write cycle, the control signals $\overline{\text{AIOWC}}$ and $\overline{\text{IOWC}}$ are activated instead of $\overline{\text{AMWC}}$ and $\overline{\text{MWTC}}$, respectively.

18.4.3 Interrupt Acknowledgement Timing

When an interrupt is received through the INTR pin of the 8086 in the minimum and maximum modes, the 8086 generates the interrupt acknowledgement ($\overline{\text{INTA}}$) signal, which we shall now discuss in detail.

When 8086 is operating in minimum mode The timing diagram for the Interrupt Acknowledgement ($\overline{\text{INTA}}$) signals of the INTR interrupt is shown in Fig. 18.12. If an INTR interrupt request has been recognized during the previous bus cycle and an instruction has just been completely executed by the 8086, a negative pulse is applied to the $\overline{\text{INTA}}$ during the current and the next bus cycles. Each of these pulses extends from T2 to T4. Upon receiving the second $\overline{\text{INTA}}$ pulse, the interface receiving the $\overline{\text{INTA}}$ signal puts the interrupt type on the lines

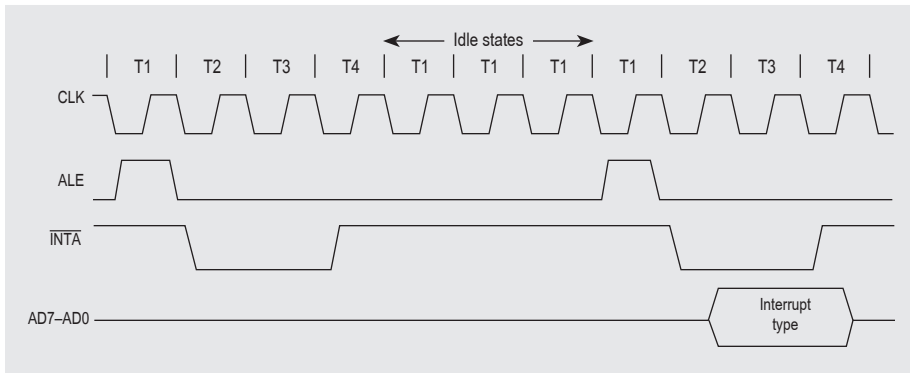


Fig. 18.12 Timing diagram for interrupt acknowledgement ($\overline{\text{INTA}}$)

AD7–AD0, which are floated for the rest of the time (during the two bus cycles). The interrupt type is available from T2 to T4.

When 8086 is operating in maximum mode In this mode, the Interrupt Acknowledgement ($\overline{\text{INTA}}$) signals are the same as in the minimum mode, but a logic 0 is applied to the $\overline{\text{LOCK}}$ pin from T2 of the first bus cycle to T2 of the second bus cycle.

18.4.4 Bus Request and Bus Grant Timing

In this section, we shall discuss the timing of a bus request and grant, both in the minimum mode and the maximum mode.

When 8086 is operating in minimum mode The timing of a bus request and a bus grant in minimum mode system is shown in Fig. 18.13. The HOLD pin is tested at the rising edge of each clock pulse. If a Hold signal is received by the 8086 before T4 or during the T1 state, the 8086 activates HLDA and the succeeding bus cycles are given to the requesting master until that master drops its request. The lowered request (i.e., HOLD = 0) is detected at the rising edge of the next clock cycle and the HLDA signal is made 0 (i.e., deactivated) at the falling edge of that clock cycle. While HLDA = 1, all the three-state outputs of the 8086 are put in their high impedance state. The instructions already in the instruction queue continue to be executed, until one of them requires the use of the bus to access the memory or the I/O device.

When 8086 is operating in maximum mode The timing of a bus request and a bus grant in a maximum mode 8086 system is shown in Fig. 18.14. A request/grant/release is accomplished by a sequence of three pulses. The $\overline{\text{RQ}}/\overline{\text{GT}}$ pins are checked at the rising edge of each clock pulse, and if a request is detected from a master such as the coprocessor and the necessary conditions discussed earlier are met, the 8086 applies a grant pulse to the $\overline{\text{RQ}}/\overline{\text{GT}}$ immediately following the next T4 or T1 state. When the requesting master receives this pulse, it takes over the control of the bus. This master may control the bus for one or several bus cycles. When it is ready to relinquish the bus, it sends the release pulse to the 8086 over the same line through which it made the request. $\overline{\text{RQ}}/\overline{\text{GT0}}$ and $\overline{\text{RQ}}/\overline{\text{GT1}}$ are the same, except that $\overline{\text{RQ}}/\overline{\text{GT0}}$ has higher priority.

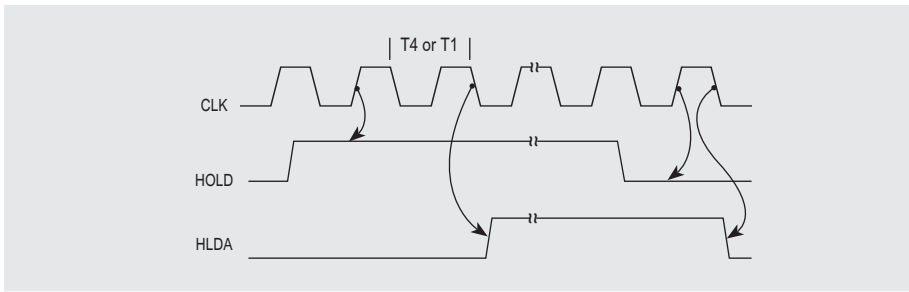


Fig. 18.13 Bus request and bus grant timing in minimum mode operation of the 8086

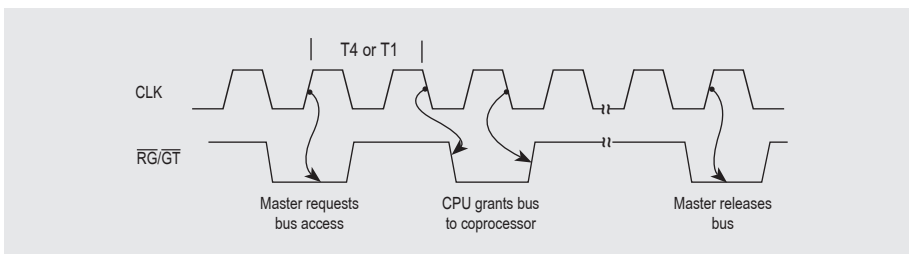


Fig. 18.14 Bus request and bus grant timing in maximum mode operation of the 8086

18.5 DESIGN OF MINIMUM MODE 8086-BASED SYSTEM

The design of a minimum mode 8086-based system requires the interfacing of memory chips and I/O devices such as DIP switches, LEDs, and 8255 with the 8086. The interfacing of memory chips and I/O devices with the 8086 has already been explained in Chapter 16. There must be a ROM/EPROM chip at the address FFFF0H, which has the monitor program stored in it, as the 8086 fetches the first instruction from that address for execution after power up and reset. In addition, there must be a ROM/EPROM or RAM chip at the address 00000H, if the system uses interrupts, as the interrupt vector table (IVT) is stored starting at that address. For interfacing the 8255 with the 8086, the concepts used to interface 8-bit I/O devices with the 8086, and the 8255 with the 8085, can be combined.

POINTS TO REMEMBER

- The 8086 can be configured to operate either in minimum or maximum mode.
- The 8284 IC (clock generator) is used to generate the clock and Ready signals for the 8086.
- The 8288 IC (bus controller) is used in the maximum mode of operation of the 8086 to generate the memory and the I/O control signals using the status signals of the 8086.
- The bus cycles of the 8086 may or may not have wait states and idle states.
- There exist different timing diagrams in the 8086, such as the timing diagram for general bus operation (i.e., the memory or I/O read cycle and the memory or I/O write cycle) of the 8086, interrupt acknowledgement, and bus request/grant in minimum and maximum modes.

KEY TERMS

Bus controller (8288) This IC is used to generate the control signals for the memory and I/O device using the status signals $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ in the maximum mode operation of the 8086.

Bus cycle Each bus cycle of the 8086 has four clock periods, T1–T4, plus any number of wait state clock cycles denoted by T_w .

Bus request/grant cycle This cycle is needed to perform the DMA operation and also when the bus is needed for another processor.

Clock generator (8284) This IC is used to supply a clock pulse with 33% duty cycle and also to synchronize the Reset and Ready signals given to the 8086.

Idle state If the bus is to be inactive or idle after the completion of a bus cycle, the gap between successive bus cycles is filled with idle state clock cycles, denoted by T1.

Interrupt acknowledgement (\overline{INTA}) cycle During this cycle, the 8086 sends two \overline{INTA} pulses to an external interface after receiving the INTR interrupt, to get the interrupt type number for the INTR interrupt.

I/O read cycle During this cycle, the 8086 reads data from the input device.

I/O write cycle During this cycle, the 8086 writes data into the output device.

Maximum mode In this mode operation, there is more than one processor, and all the control signals for the memory and the I/O device are generated by the bus controller (8288) chip.

Memory read cycle During this cycle, the 8086 reads data or instructions from the memory.

Memory write cycle During this cycle, the 8086 writes data into the memory.

Minimum mode In this mode operation, there is only one 8086 processor, and all the control signals for the memory and the I/O device are generated by the processor itself.

Wait states These states are inserted between T3 and T4, when a memory or I/O interface is not able to respond quickly enough during a data transfer. This is achieved with the help of the Ready input in the 8086.

REVIEW QUESTIONS

1. What is meant by minimum mode operation of the 8086?
2. What is meant by maximum mode operation of the 8086?
3. What is the function of the $\overline{MN}/\overline{MX}$ pin in the 8086?
4. How are the control signals \overline{MEMR} and \overline{MEMW} generated using the $\overline{M}/\overline{IO}$, \overline{RD} , and \overline{WR} signals in the minimum mode operation of the 8086?
5. How are the control signals \overline{IOR} and \overline{IOW} generated using the $\overline{M}/\overline{IO}$, \overline{RD} , and \overline{WR} signals of the 8086?
6. What is the function of the chip select logic and what are the inputs given to it?
7. Write the function of the clock generator IC (8284).
8. What is the role of the bus controller IC (8288)?
9. What is meant by memory read and memory write cycles?
10. What is meant by I/O read and I/O write cycle?
11. Write the function of the signals \overline{DEN} and $\overline{DT}/\overline{R}$ in the 8086.
12. What is the function of the signals $\overline{M}/\overline{IO}$ and \overline{BHE} in the 8086?
13. What is the role of the pin $\overline{F}/\overline{C}$ in the 8284A?

14. Explain the minimum mode configuration of the 8086-based system with the necessary block diagram.
15. Describe the maximum mode configuration of the 8086 with the necessary block diagram.
16. Explain the signals in the 8284A and the 8288 in detail.
17. Explain the bus timings for general bus operation in the 8086 under minimum mode with necessary waveforms.
18. Explain the bus timings for general bus operation in the 8086 under maximum mode with necessary waveforms.
19. With necessary waveforms, describe the bus timings for bus request and grant in minimum and maximum modes.
20. How does the 8086 respond to the INTR interrupt in minimum mode operation of the 8086?

THINK AND ANSWER

1. How are wait states introduced in a bus cycle of the 8086?
2. Why and when are the idle states introduced in a bus cycle of the 8086?
3. How many clock periods are present in a bus cycle of the 8086 without wait states?
4. What is the difference between the \overline{AMWC} and \overline{MWTC} signals?
5. How does the 8288 generate the control signals for memory and I/O devices?

NUMERICAL/DESIGN-BASED EXERCISES

1. Design an 8086-based minimum mode system that contains the following components:
 - (a) Two $8K \times 8$ EPROM chips having the address range FC000H–FFFFFH
 - (b) Two $8K \times 8$ RAM chips having the address range 80000H–83FFFH
 - (c) Two seven-segment LEDs with common anode connection, having the addresses 80H and 81H
 - (d) An 8-bit DIP switch having the address FF80H
2. Interface an 8255 chip with the 8086 operating in minimum mode so that the addresses 80H, 81H, 82H, and 83H are assigned to port A, port B, port C, and the control register of the 8255, respectively.